



Efficient ATFA design based on CNTFET technology for error-tolerant applications

Rabe'e Sharifi Rad¹ · Mokhtar Mohammadi Ghanatghestani² · Malihe Hashemipour¹

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Abstract

Today, the main concern of digital circuit designers is reducing the power of portable equipment due to the limitation of charging their batteries. One of the ways to reduce power consumption is to use approximate units in systems that have the ability to tolerate faults. Another solution to consider is designing circuits with Multi-Valued Logic (MVL), which can also reduce power consumption. The use of CNTFET transistors in MVL circuit designs can lead to higher efficiency in integrated circuits, particularly in terms of power, speed and area. Full adders are essential arithmetic modules in processors and serve as the cornerstone of digital systems. In this research study, we aimed to design an Approximate Ternary Full Adder (ATFA) with the minimum number of transistors and power consumption. Based on simulations conducted using Synopsys HSPICE in Stanford's 32 nm CNTFET technology, the proposed ATFA design demonstrated superior performance compared to previous similar designs, particularly in terms of average power consumption, delay, and energy consumption. In addition, according to the examination of noise immunity curves, the proposed circuit has higher pulse noise amplitude in all pulse widths than other circuits. Meanwhile, at the program level, image composition has been considered to study accuracy criteria such as peak Signal-to-Noise Ratio (PSNR), Structural Similarity (SSIM), and Figures Of Merit (FOM) in image synthesis, supported the superior performance of our proposed circuit compared to other similar circuits.

✉ Mokhtar Mohammadi Ghanatghestani
mokhtarmohamadi@srbiau.ac.ir

Rabe'e Sharifi Rad
rabeesharifi@iauk.ac.ir

Malihe Hashemipour
m.hashemi@iauk.ac.ir

¹ Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran

² Department of Computer Engineering, Bam Branch, Islamic Azad University, Bam, Iran

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1 Introduction

Nowadays, the design of digital circuits has become one of the most important technological challenges due to the increasing demand for the use of portable equipment and the limited ability to charge their batteries continuously. Therefore, reducing power consumption in the design of nano-electronic circuits is critical to the efficiency of digital circuits. A significant part of the power consumption in portable devices such as mobile phones, laptops, and medical sensors is related to digital circuits, particularly digital signal processing and complex calculations [35, 43].

Recently, there has been a trend to use portable electronic devices that can be charged quickly, even at a high rate of power consumption [29]. Precise calculations often involve many complexities, making them a key issue in designing digital circuits. One potential solution to reduce the complexity of calculations with the aim of reducing power consumption in digital circuits is to use approximate calculations that are fault-tolerant [24].

It appears that CMOS technology is approaching the end of its technological roadmap, as it faces significant problems such as short-channel effects, high leakage power, reduced gate control, parametric changes, and higher power density, as well as increasing the cost of nanoscale lithography. Most importantly, heat production is a significant concern, as it can seriously degrade circuit performance and cause failure [33].

To overcome these issues related to CMOS circuits, the use of nano-technologies is being proposed as a viable alternative. Carbon nano-transistors are the most promising technology among them. Additionally, Multi-Valued Logic (MVL) can replace binary logic, allowing for more than two logic levels to be employed. MVL has several advantages over binary logic, including increased efficiency in computing operations, reduced wire connections, and a reduction in the area and power consumption of the chip. As a result, the design of multi-valued circuits using carbon nanotube transistors has generated significant interest [2, 32, 42, 44].

CNTFETs offer several advantages compared to MOSFETs. Firstly, CNTFETs are faster due to the enhanced carrier mobility of carbon nanotubes, resulting in improved switching speed and signal processing. Secondly, CNTFETs consume less power due to reduced leakage currents and power dissipation, making them more energy-efficient, especially in high-performance applications. Additionally, CNTFETs exhibit better temperature resilience due to their high thermal conductivity. Furthermore, CNTFETs enable improved device scaling and miniaturization, making them suitable for advanced nano-electronic circuits. These advantages position CNTFETs as a promising alternative to MOSFETs in various applications [31, 40].

To create multi-valued circuits, designers carefully adjust the diameter of the nanotube and produce transistors with different voltage thresholds throughout the circuit

design process. Adjusting different threshold voltages is the most important feature of carbon nanotube transistors that can facilitate this process.

By incorporating approximate calculations into circuit design, the complexity of the circuit design can be significantly reduced. However, it is vital to consider the error tolerance in the designed circuit. The maximum error tolerated in digital systems may reduce the quality of overall processing to some extent, but this remains acceptable depending on the intended output application, and it does not compromise the system performance. Other factors driving the adoption of approximate circuit design include an increase in data processing volume and the need for faster processing speeds. Generally, using approximate calculations in circuit design helps to minimize power consumption and delay, resulting in improved efficiency across different abstract levels.

As mentioned, using approximate units in systems that are fault-tolerant is a method to reduce power consumption and increase the efficiency of digital circuits. Although it reduces the quality of the overall processing to some extent, it does not lead to large errors and can be used in applications such as graphics or wireless communications.

Because adders are the most important arithmetic modules in processors, they form the basis of digital systems. So, power reduction in them causes power reduction in other computing units, such as sub-tractors, multipliers, dividers, and Arithmetic Logic Units (ALUs), and saves power. Therefore, it is important to design approximate adders that have low power consumption and high computing speed to increase the efficiency of the entire digital system [18, 31, 40, 44].

Improving the power consumption, delay, and efficiency of a digital system can be done at different abstract levels such as algorithm [39], architecture [27], gate [1], and transistor [11].

One of the ways to reduce power consumption is to use approximate units in systems that have fault tolerance. Therefore, approximate units can be used in applications such as graphics or wireless communication. The use of approximate computing units with acceptable accuracy reduces the quality of the overall processing to some extent but does not cause large errors. Because adders, as the most important arithmetic modules in processors, are the basis of digital systems, and power reduction in them cause's power reduction in other computing.

Due to the importance of the subject, the Full Adder cell has been designed for minimum power consumption. Additionally, to achieve energy efficiency in the proposed Full Adder, we have used approximate calculations, Ternary Logical, and carbon nanotube transistors. In the following sections, in the following sections, we compare the proposed ATFA with other approximate ternary full adders designed in [10, 21, 28], as well as exact full adders in [20, 46].

In the remainder of the paper, Sect. 2 briefly describes the background of the research in three parts. The first part covers carbon nanotube field-effect transistors, the second part covers approximate calculations, and the third part covers Multi-Valued Logic (MVL). In Sects. 3 and 4, we present the proposed ATFA and discuss performance and simulation results and comparisons at the circuit and application level. The overall conclusion is presented at the end of the paper.

2 Backgrounds of Research

2.1 Carbon Nanotube Field Effect Transistors

In 1991, Carbon NanoTube (CNT) was discovered accidentally by Iijima [19]. It refers to an allotrope of carbon atoms that has unique mechanical and electrical properties, making it an excellent conductor of electricity and heat. A CNT is formed when a graphene sheet is rolled into a one-dimensional hollow cylinder around a center [9]. There are two types of CNTs, Single-Walled CNTs (SWCNTs) and Multi-Walled CNTs (MWCNTs) that have different characteristics [3, 47]. MWCNTs were discovered earlier than SWCNTs [41].

Despite the conductor nature of graphene sheet according to the chiral vector, SWCNTs can work as semiconductors or conductors. The chiral vector is determined by the vector around which the graphene sheet is rolled, fixing the angle of the carbon atoms along the length of the nanotube. This vector is defined by Eq. 1 [5]:

$$\vec{C}_h = n_1 \vec{a}_1 + n_2 \vec{a}_2 \quad (1)$$

SWCNTs are classified into three general groups based on their chiral number: armchair ($n_1 = n_2$), zigzag ($n_1 = 0$ or $n_2 = 0$), and chiral (all other indices) (Chiral angle (θ) and chiral numbers (n_1, n_2)). The chiral number determines whether the nanotube is conductive or semi-conductive. If $n_1 - n_2 = 3k$ (where $k \in \mathbb{Z}$), the nanotube is conductive; otherwise, it is semi-conductive [5]. As a result, armchair-structured nanotubes are conductive, while zigzag-structured nanotubes are semi-conductive [5, 25]. The gate width of a CNTFET can be calculated using Eq. (2) [4]:

$$W_{\text{gate}} = \text{Max} (W_{\text{min}}, (N - 1) \text{Pitch} + D_{\text{CNT}}) \approx N \cdot \text{Pitch} \quad (2)$$

where W_{min} is the minimum possible width for the gate, which is determined, based on lithography limitations, N is the number of nanotubes under the gate, and Pitch is the center distance of two adjacent nanotubes under a gate.

The length of the chiral vector is equal to the perimeter of the cross section of the nanotube. This length is divided by π times the diameter of the nanotube, which is very effective in determining its properties. because by changing the nanotube diameter, different threshold voltages are obtained, which is useful in the design of Multi-Valued Logic (MVL) circuits and is calculated from Eq. (3) and determines the energy gap of the intrinsic semiconductor nanotube through Eq. (4), where $V\pi$ (3.033 eV) is the carbon π - π bond energy [4].

$$D_{\text{CNT}} = \frac{C_h}{\pi} = \frac{\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \approx 0.0783 \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (3)$$

$$E_g = \frac{2\sqrt{3}}{3} \frac{aV\pi}{D_{\text{CNT}}} \approx \frac{0.86}{D_{\text{CNT}}(\text{nm})} eV \quad (4)$$

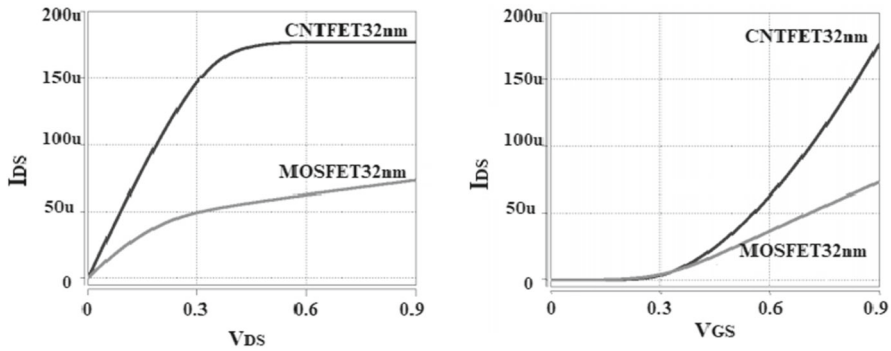


Fig. 1 The current–voltage (I–V) characteristics of MOSFET and CNTFET of the same dimensions

The threshold voltage is approximately half of the band gap and is calculated by Eq. (5) [36].

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aE_\pi}{D_{CNT}} \approx \frac{0.43}{D_{CNT}} \quad (5)$$

The current–voltage (I–V) characteristics of MOSFET and CNTFET devices are presented in Fig. 1. In 32 nm technology, a CNTFET exhibits a suitable current–voltage characteristic without short-channel effects, while a MOSFET in 32 nm technology does not have such high channel resistance. As a result, CNTFET has significantly higher conductivity compared to MOSFET, and in MOSFET, the carrier velocity decreases at high gate–source voltages at the channel level, leading to reduced conductivity [16].

The similar current–voltage (I–V) characteristic and the existence of two types of P and N transistors in both MOSFET and CNTFET transistors have made the latter a suitable alternative to the former. This type of CNTFET has been utilized to design digital circuits with impressive efficiency in terms of structure and intrinsic and functional characteristics, which resemble those of MOSFET despite the same drive capability of P and N transistors in CNTFET and their identical geometries and movements ($m_n = m_p$) [30].

In this article, the design of the proposed ATFA was focused on achieving high efficiency using a CNTFET like MOSFET based on the aforementioned characteristics [30].

2.2 Review of Ternary Logic Design

With the emergence and development of semiconductor elements, multi-valued semiconductor circuits were designed and used at the same time as two-valued semiconductor circuits. But two-valued logic has expanded significantly in recent decades due to the efficiency in operating systems and two-mode microelectronics. On the other hand, the binary system has challenges such as high implementation space for

micro-communications, increasing the heat generated and power consumption. To solve this problem, Multi-Valued Logic has been introduced [34, 42].

It was mentioned in the introduction that multi-valued logic has significant advantages that make it suitable for low-power design. Besides the advantages available for multi-valued circuits, one of their challenges is how to implement and coordinate with binary systems and technologies, which must be considered [8].

The use of CNTFET transistors solves part of the challenges of multi-valued logic due to their multi-threshold design. In the design of MVL circuits, the optimal radix is equal to e , but due to hardware limitations, the radix must be a natural number, among which the use of a radix of three, which is the closest integer to the optimal root, is the most efficient situation [15]. So in this research, Ternary logic is used and has three logic levels for which there are equivalent voltages. The three logic levels and their corresponding voltages are listed below:

logical level	'0'	'1'	'2'
voltage	'GND'	'Vdd/2'	'Vdd'

2.3 Approximate Computing

Approximate computing is a design approach for developing high-performance electronic circuits that trade computational accuracy for decreased power consumption and delay [26]. While these circuits may occasionally produce incorrect results, they simplify circuit designs and are widely utilized in applications such as image processing, signal processing, multimedia processing, and machine learning. It is critical to consider the type of data being processed and the acceptable error tolerance while employing approximate calculations. Using approximate calculations for control systems can have severe consequences, making it crucial to limit their usage to non-critical data [23, 45].

Signal processing, especially for image and video processing, can benefit from approximate calculations since the limitations of human vision allow for imprecision while still providing satisfactory results. Approximate calculations can be applied at any stage of circuit design, including algorithm selection and hardware circuit designing [17]. Given these benefits, it is crucial to evaluate the output produced by circuits generated using approximate calculations to ensure their quality and accuracy. This can be accomplished by considering several error parameters such as MED, NED, PSNR, and MSSIM presented in Table 1. Although ED is commonly used for evaluation, it may not always be enough to determine the output's overall quality. Thus, it is important to incorporate PSNR and MSSIM parameters, as they provide a more in-depth analysis of the output's accuracy. By thoroughly analyzing the output, the benefits of approximate calculations can be maximized while reducing the risk of errors or inaccurate results, particularly in data-critical systems. Sections 4 provides detailed descriptions of PSNR and MSSIM parameters for the analysis.

Table 1 Error evaluation parameters

Error Metric	Description	Equation	Equation No
ED	Error Distance	$ s - s' $	(6)
MAE	Maximum Error Distance	Maximum (ED)	(7)
TED	Total error distance	$TED = \sum_{i=1}^N ED$	(8)
MED	Mean error distance	$MED = \frac{TED}{N}$	(9)
NED	Normalized mean error distance	$NED = \frac{MED}{N}$	(10)

3 Proposed Design

The ATFA cell has been designed with an efficient parallel structure that incorporates approximate calculations to reduce its delay and power consumption. The design utilizes a multiplexer and TGate and begins by accurate calculation of the sum of two bits with a ternary half-adder cell [22]. Next, the output values of the full adder for the Sum and Cout bits are determined in parallel based on the value of the Cin input bit. The ATFA output has two states based on the value of Cin. When Cin is equal to 0, the output of the half-adder is the same as the ATFA output, resulting in an exact output without errors. In this case, the output of ATFA is $a + b + 0$, where the circuit produces no errors. The second state arises when the output of ATFA is approximate and may have errors in some cases, which is calculated according to the value of Cin. If Cin equals 1, the result of ATFA is $a + b + 1$, and if Cin equals 2, $a + b + 2$ is transferred to the output of ATFA. In cases where Cin is nonzero, the values of Sum and Cout may be approximated and have errors.

To gain a better understanding of the ATFA, refer to Fig. 2, which shows the block diagram of the ATFA. The diagram demonstrates the data flow after $A_i + B_i$ is calculated using a triple half-adder, setting the output bits Sum + 0 and Cout + 0. Parallel operations are then performed to determine the values of Sum + 1, Sum + 2, Cout + 1, and Cout + 2. The design incorporates a base multiplexer, with Sum + 0, Sum + 1, and Sum + 2 as multiplexer D inputs and Cout + 0, Cout + 1, and Cout + 2 as inputs of the multiplexer E. The output of the ATFA is determined by the value of Cin assigned to the multiplexer selector. If Cin equals 0, the input number zero of multiplexer D and E is placed in the output, producing Sum + 0 and Cout + 0, respectively. Note that all calculations are performed independently and in parallel, and the final output is determined based on the value of Cin.

This section presents Table 2, which is the ATFA truth table, comparing it to Table 3, which is the exact truth table of a ternary full adder. The bold digits in Table 2 and Table 3 show the situations in which errors occurred.

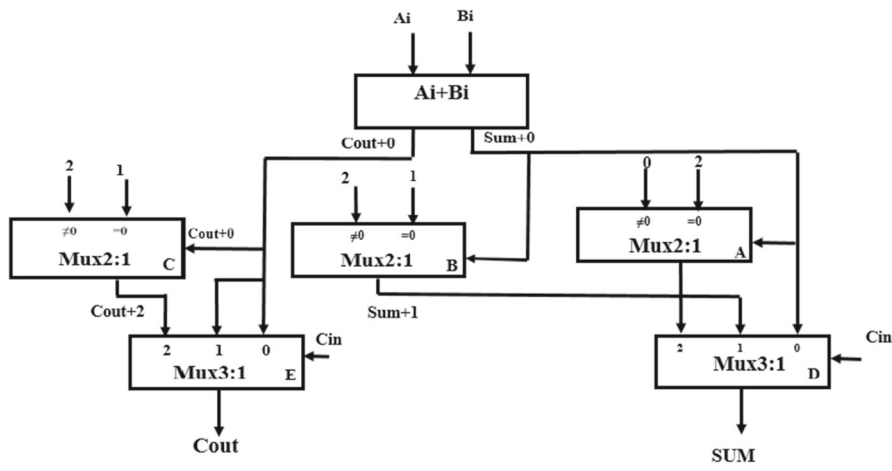


Fig. 2 The First ATFA block diagram

Table 2 The ATFA truth table (APPROXIMATE)

CIN value	CIN = 0		CIN = 1		CIN = 2	
	Cout	Sum	Cout	Sum	Cout	Sum
$\sum IN$						
0	0	0	0	1	0	2
1	0	1	0	2	1	0
2	0	2	1	0	1	1
3	1	0	1	1	1	2
4	1	1	1	2	2	0

Table 3 The TFA truth table (exact)

CIN Value	CIN = 0		CIN = 1		CIN = 2	
	Cout	Sum	Cout	Sum	Cout	sum
$\sum IN$						
0	0	0	0	1	1	2
1	0	1	0	2	1	0
2	0	2	0	2	1	0
3	1	0	1	1	2	2
4	1	1	1	2	2	0

According to Table 2, Eqs. (11–14) are used to calculate the sum and Cout in the approximate full adder. Equation (9) is used when $C_{in} = 1$, and Eq. (10) is used when $C_{in} = 2$.

$$Sum_{+1} = \begin{cases} 1 & Sum_{+0} = 0 \\ 2 & Sum_{+0} \neq 0 \end{cases} \quad (11)$$

$$Cout_{+1} = Cout_{+0} \quad (12)$$

$$Sum_{+2} = \begin{cases} 2 & Sum_{+0} = 0 \\ 0 & Sum_{+0} \neq 0 \end{cases} \quad (13)$$

$$Cout_{+2} = \begin{cases} 1 & Cout_{+0} = 0 \\ 2 & Cout_{+0} \neq 0 \end{cases} \quad (14)$$

The present work describes an approach to reduce circuit area and power consumption so by revisiting the input values of all multiplexers in the circuit. Specifically, these input values are determined based on the $Cout + 0$, $Sum + 0$, and fixed values. By applying this method, the multiplexer A can be replaced with an NTI circuit, as its similar logic function to the NTI inverter allows for a reduction in both circuit area and power consumption. Similarly, the input values of multiplexer E are shown to have an identical input, which enables its replacement with a 2:1 multiplexer. These changes, depicted in the ATFA block diagram, have enhanced the circuit design and can lead to improved overall system functioning. It is noteworthy that the adoption of methods such as these is necessary for modern computing systems, whereby achieving the optimal balance between circuit area and power consumption is a significant concern. Figure 3 provides a visualization of the recent changes made to the ATFA block diagram, demonstrating the efficacy of this approach in achieving these goals.

The proposed ATFA cell provides a comprehensive solution to functionally improve ternary arithmetic systems. The ATFA cell consists of A ternary half-adder cell [25], three 2-to-1 multiplexers, including multiplexers C, B, and E, which produce $Cout + 2$, $Sum + 1$, and $Cout$, respectively. Additionally, a 3-to-1 multiplexer named D is included to determine the output value of Sum . The design of the full ternary adder leverages pass transistors and transfer gates, which reduce the hardware level of the circuit.

The implementation of multiplexer circuit B is shown in Fig. 4, which generates $Sum + 1$, has fixed inputs and utilizes a selector connected to $Sum + 0$, as indicated by Table 2 and Eq. (9). If $Sum + 0$ is equal to zero, the output of multiplexer B generates one, and if not, generates two, which may result in errors in specific input states. Multiplexer D is responsible for the output of Sum and connects $Sum + 0$, $Sum + 1$, and $Sum + 2$ as its inputs, with C_{in} as its selector.

To achieve the desired output, the threshold voltage value for transistors T1 and T4 in the multiplexer circuit B is selected. Specifically, the T1 transistor is activated by logic two, while transistor T4 is activated with logic zero or one. The threshold voltage values of transistors T2 and T3 follow normal conventions.

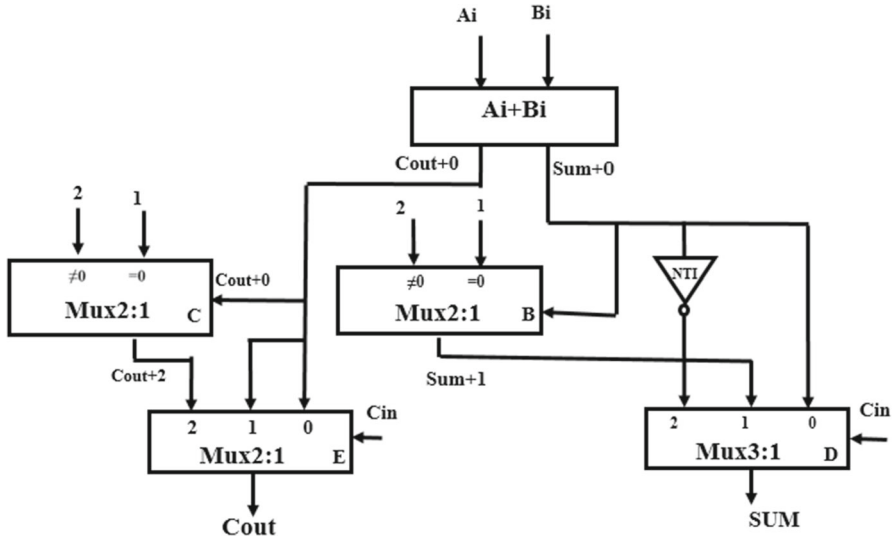
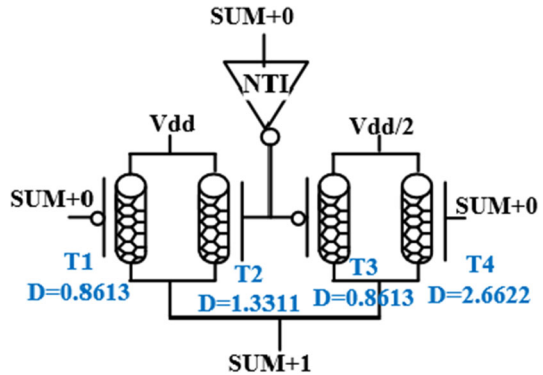


Fig. 3 The Second ATFA block diagram

Fig. 4 Multiplexer B



Multiplexers C and E, which are responsible for generating Cout, are designed with a similar approach as multiplexer B. Specifically, multiplexer C utilizes a selector connected to Cout + 0, as demonstrated by Table 2 and Eq. (12). If Cout + 0 = 0, the output of multiplexer C generates one, and if not, generates two (Cout + 2 = 2).

The inputs to multiplexer E are Cout + 0 and Cout + 2, with Cin as the selector. A 2-to-1 multiplexer may be used instead of a 3-to-1 multiplexer in the design of the ATFA cell to reduce the number of transistors when Cout + 1 = Cout + 0, which is outlined by Eq. 10. This replacement leads to a reduction in the area of the ATFA. Multiplexer E generates Cout. When Cin = 2, the output of multiplexer E is Cout + 2, and when Cin is not equal to 2, the output is Cout + 0.

In Fig. 5, the implementation of multiplexer D is depicted. In this figure, certain transistors, such as T1, T3, T5, and T8, possess a shared threshold voltage. However,

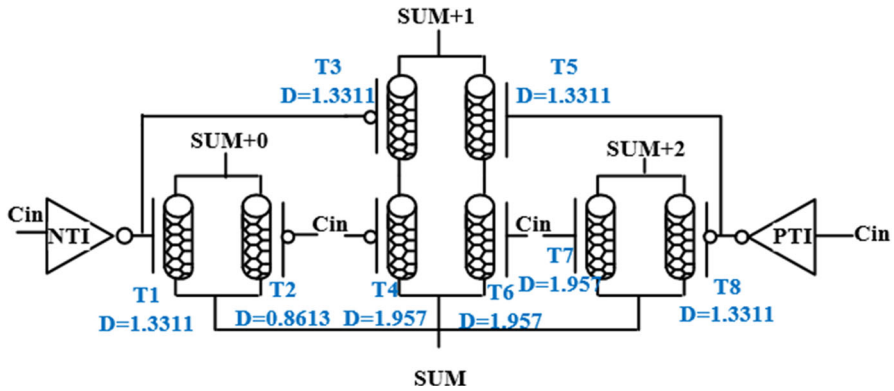


Fig. 5 Multiplexer D

to generate the desired output of the ATFA circuit, separate threshold voltage values are chosen for transistors T2, T4, T6, and T7. Specifically, T2, T4, and T7 are activated for logic zero and logic zero or one inputs, as well as logic two inputs, respectively. In contrast, T6 is enabled for logic zero or two inputs. Figure 6 offers the complete representation of the ATFA circuit implementation.

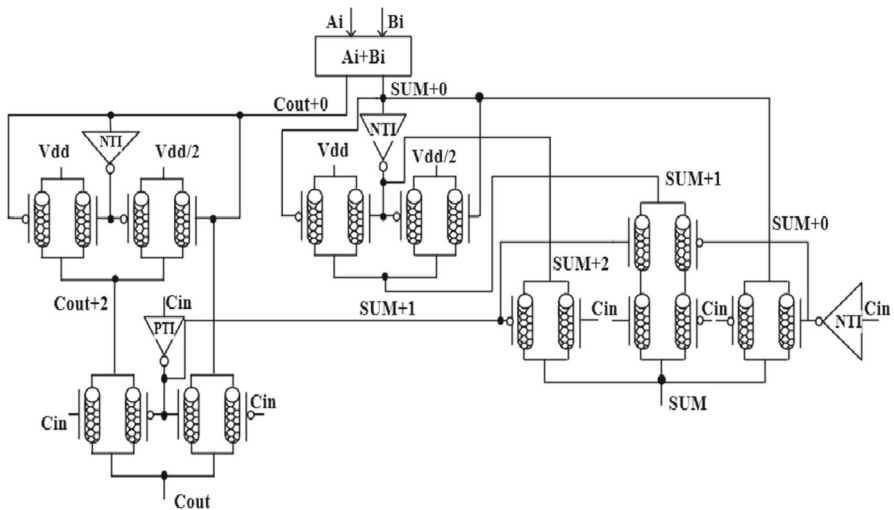


Fig. 6 The complete ATFA circuit

4 Simulation

To assess the efficiency of the ATFA circuit, the Synopsys HSPICE simulation software was utilized to evaluate its performance relative to similar circuits designed previously. The study considered several performance metrics, including power, delay, and PDP, across different conditions. The comprehensive SPICE 32 nm Stanford CNT-FET model was used as a standard for CNTFET devices, and important CNTFET parameters and values were shown in references [6, 7].

This model has become the standard for CNTFET devices. Important CNTFET parameters and their values are shown in Table 4 with brief descriptions [6, 7].

The simulations took place at room temperature. After considerable simulation, the proposed ATFA circuit, which had a frequency of 0.9 V and 250 MHz with a 2.1 fF load capacity, underwent PDP and EDP optimizations, with the resulting optimized waveform being presented in Fig. 7.

The proposed ATFA, along with three previously designed ATFAs, underwent simulations under the same conditions, at a frequency of 0.9 V and 250 MHz and a temperature of 27 °C with a load capacity of 2.1 fF, and the simulation results are presented in Table 5.

Three diagrams of delay, power, and PDP were generated to display the simulation results of the proposed ATFA and the circuits in Table 5 at supply voltages of 0.7, 0.8, and 0.9 V, with other parameters remaining constant, as shown in Fig. 8.

According to the simulation results under the same conditions, the proposed ATFA exhibited significantly lower delay times than the other three ATFAs. This can be attributed to the parallel circuit design, which has a much shorter critical path than the previous circuits. Further evidence of its efficiency is recorded in the simulation results of EDP. The number of transistors used in the design of this circuit led to a significant reduction in proposed ATFA's area. It is important to stress that the improvement of ATFA efficiency extends beyond delay reduction and area limitation, as the circuit's total switching capacity is less, power consumption is decreased, and the best PDP has been achieved.

Table 4 CNFET Model Parameters

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of the doped CNT source-side extension region	32 nm
L_{dd}	The length of the doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20pF/m
E_{fi}	The Fermi level of the doped S/D tube	6 eV

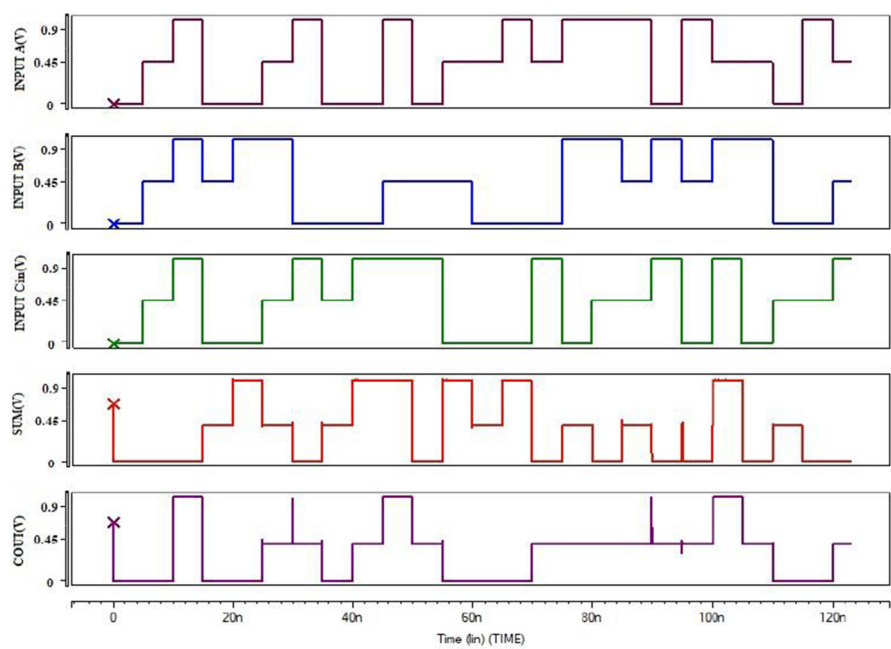


Fig. 7 Input and output waveform snapshots of the proposed design

Table 5 Comparison of Ternary Full Adders

TFA	Delay (E-12)	Power (E-06)	PdP (E-17)	EDP (E-32)	The number of transistor
proposed ATFA	8.06135	11.6250	9.37132	7.55454	48
ATFA1 in [28]	32.9699	24.5164	80.8305	266.498	97
ATFA2 in [28]	33.5630	24.5775	82.4897	276.861	115
ATFA in [10]	16.7650	23.3963	39.2239	65.7588	82
ATFA2 in [21]	9.95720	17.9154	17.8387	17.7623	64
TFA in [46]	351.798	1.88630	66.3597	2334.52	66
TFA in [20]	79.5291	19.8386	157.775	1254.76	31

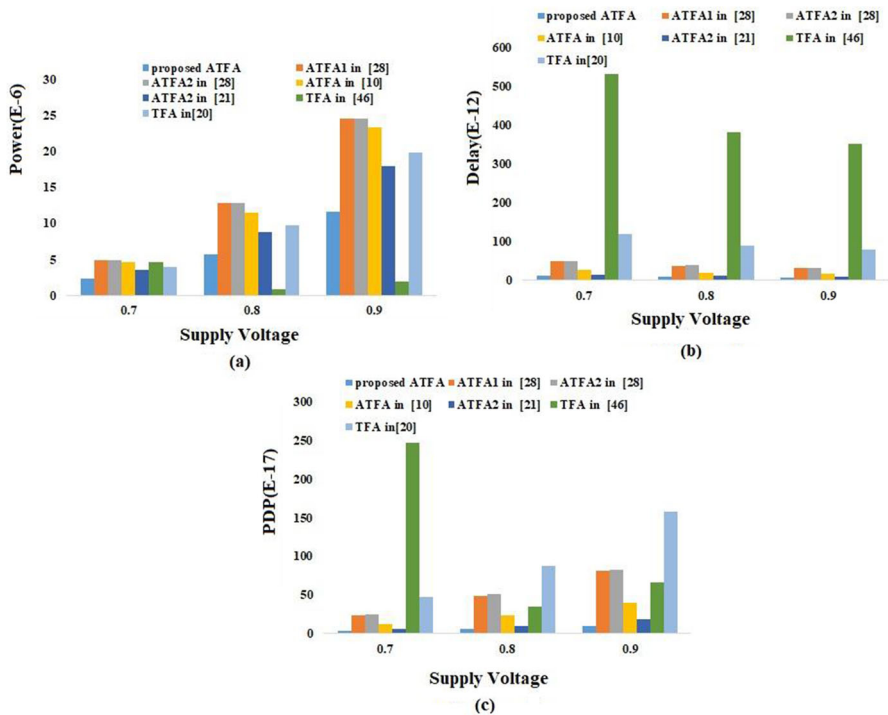


Fig. 8 ATFAs Diagram at different voltages, **a** Power consumption. **b** Delay. **c** PDP

Based on the results, the proposed design demonstrates significantly lower delay and power delay product compared to the other three approximate ternary full adders based on CNTFETs. It is more evident that the proposed approximate adders are more efficient, attributed to several factors such as fewer transistors, a simpler structure, a smaller total switching capacity, and a shorter critical path than previous circuits. Table 5 presents the total number of transistors in all circuits, with the proposed design occupying significantly less area due to its smaller transistor count. As it is obvious, the proposed design demonstrates the best PDP and delays when compared to other cells under the same conditions, utilizing the least number of transistors in its design.

The simulation of different load capacitor sizes is presented in Table 6 and shows the performance parameters of the circuit, such as delay and power consumption, based on different load capacitors.

Table 6 The simulation of different load capacitor

Load Capacitor	Delay(E-12)	Power(E-06)	PdP(E-17)
2fF	8.06135	11.6250	9.37132
3fF	16.5685	11.7698	19.5007
4fF	37.7053	11.7848	44.4349
5fF	58.0683	12.0831	70.1645
6fF	81.7431	12.2185	99.8778

Table 7 The simulation of different temperature

Temperature	Delay(E-12)	Power(E-06)	PdP(E-17)
0	8.0037	11.843	9.4788
10	8.0124	11.842	9.4884
20	8.0527	11.624	9.3604
30	8.0614	11.625	9.3714
40	8.9313	11.987	10.706
50	9.1058	12.546	11.424
60	11.122	12.890	14.337
70	12.892	13.653	17.602

The circuits underwent extensive simulations across a broad temperature range of 0 to 70 °C to assess their susceptibility to temperature variations. The outcomes from this experimental study, conducted with a supply voltage of 0.9 V, a frequency of 250 MHz, and a load capacitance of 2.1 fF, are represented in Table 7.

4.1 Monte Carlo Simulation

The Monte Carlo simulation is a widely adopted statistical technique that leverages sampling to estimate solutions to quantitative problems. By portraying uncertainty, the method helps organizations better understand the potential that exists within their business or system and make informed, data-driven decisions. To determine the stability of the ATFA cells when faced with variations in the carbon nanotube diameter, a Monte Carlo analysis was conducted, which incorporated a Gaussian distribution with a 6-sigma range. The primary goal of this analysis was to assess the ATFA circuit’s robustness. Through running simulations 30 times, the team ensured at least 80% of the circuit’s components could demonstrate satisfactory performance, with a 99% probability [37]. The mean (μ), variance (σ^2), and standard deviation (σ) were then considered as indicators for the circuit’s capacity to withstand variations in the manufacturing process [38], which ranged from 0.05 to 0.2 nm away from the average value. The analysis considered these manufacturing process variations to provide a comprehensive understanding of the circuit’s resilience.

$$\mu = \frac{x^1 + x^2 + \dots + x^n}{N}$$

(15)

$$\sigma^2 = \frac{(x_1 - \mu)^2 + (x_2 - \mu)^2 + \dots + (x_n - \mu)^2}{N - 1}$$

(16)

$$\sigma = \sqrt{\sigma^2}$$

(17)

In formulas 15, 16, 17, xi represents the values of the variables and N represents the number of iterations. For these simulations, we assumed the value of N to be 30. The simulation results in Table 8 demonstrate that the proposed design provided good

Table 8 Mean, variance, and standard deviation values of the proposed cell against diameter deviations

Diameter Deviations (nm)	0.05	0.10	0.15	0.20
<i>Mean (μ)</i>				
Power (E-6 W)	3.215	3.217	3.213	3.215
Delay (E-12 S)	12.17	12.19	12.31	12.52
PDP (E-17 J)	3.912	3.921	3.955	4.025
<i>Variance (σ^2)</i>				
Power (E-16 W)	0.5396	0.6267	0.8046	0.8939
Delay (E-26 S)	0.5234	1.2818	1.7279	2.1794
PDP (E-36 J)	0.2824	0.8034	1.3903	1.9483
<i>Standard deviation (σ)</i>				
Power (E-8 W)	0.7346	0.7917	0.8970	0.9455
Delay (E-13 S)	0.7235	1.1322	1.31451	1.4763
PDP (E-18 J)	0.5314	0.8963	1.1791	1.3958

performance. We found that after 30 repetitions, it consistently produced accurate and stable results despite changes in the diameter of carbon nanotubes.

4.2 The layout of Circuit

Layout design is a crucial step in electronic circuit design. The process of layout design is a fundamental aspect of electronic circuit design that plays a critical role in estimating the circuit's area.

As discussed in the previous sections, the proposed ATFA design utilizes a reduced number of transistors compared to other ATFAs, as indicated in Table 5. In this study, the physical design tool of CNTFET circuits, as outlined in [12–14], was employed to generate the layout of the proposed ATFA. The layout is portrayed in Fig. 9. Subsequently, we used the physical design tool mentioned above to create a layout that represents the circuit and estimate the area of the proposed approximated ternary full adder circuit.

4.3 Noise Immunity Analysis

The study presented in Fig. 10 displays noise immunity curves that demonstrate a circuit's capacity to withstand noise without compromising its functionality. These curves also indicate that circuits are susceptible to incorrect output when subjected to noise, which can negatively impact the quality of the circuit's performance. Therefore, vital information on a circuit's immunity to various noise sources can be gathered by analyzing Noise Immunity Curves (NIC). When generating these curves, the circuit

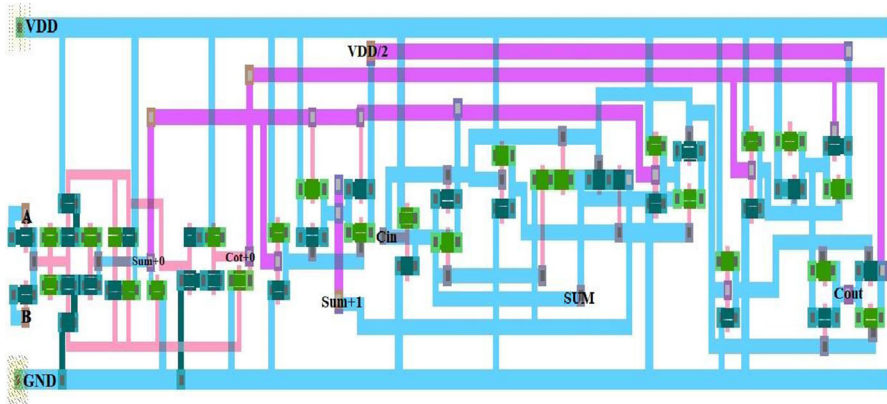


Fig. 9 The layout of the proposed design

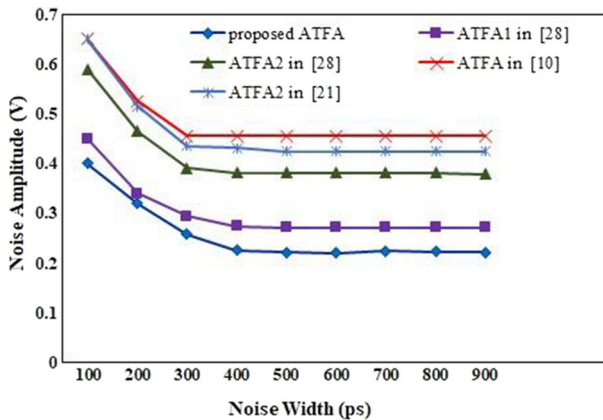


Fig. 10 ATFAs Noise immunity curves

gets subjected to noise input via an adjustable noise injection circuit while restricting the other inputs. The curves derived from this analysis can detect dangerous areas above each curve of the circuit, as well as the safe area beneath the curve.

NIC curves can determine a circuit's unreliability by evaluating the circuit's noise immunity threshold. Typically, circuits with higher NIC curves exhibit better noise immunity. The proposed ATFA design exhibited superior noise immunity capabilities when compared to other ATFAs. Results revealed higher pulse noise amplitude at all pulse widths, providing evidence of the design's reliable output even when exposed to noise. Therefore, NIC curves can provide essential insights for circuit designers and developers in producing practical, reliable, and robust circuits that can withstand real-world conditions.

4.4 Error Evaluation Parameters

To evaluate the error parameters of the proposed ATFA circuit, it is necessary to calculate the Maximum Error Detected (MED) and Number of Errors Detected (NED) parameters. Table 2 and Table 3 in the previous sections provide input combinations that trigger an error in both the Cout and Sum outputs. Based on this information, Table 9 can be utilized to identify the input combinations that result in output errors. From this, we can calculate the MED and NED values using Eqs. (18, 19, and 20) for each output. By conducting this analysis, we can identify the circuit’s performance thresholds. Additionally, detecting the input combination that generates errors enables us to pinpoint the source of the error and subsequently rectify the identified faults.

To assess the trade-off between the circuit’s accuracy criteria and analysis parameters, Table 10 reports the product of NED in power, NED in power and delay, NED in power, delay, and total power dissipation and NED in delay and power. There is another parameter called PDANEDP that depends on power, delay, area, and NED of all ATFAs in Table 10. The proposed ATFA design showed better results across all parameters in Table 10 except for one, indicating that the trade-off between accuracy

Table 9 Cout and Sum output error values of the proposed method

ABCi	Cout (exact)	Cout (approximate)	Error Cout	SUM (exact)	SUM (approximate)	Error SUM
111	1	0	− 1	0	2	− 2
201	1	0	− 1	0	2	− 2
021	1	0	− 1	0	2	− 2
002	0	1	1	−	−	−
122	2	1	− 1	−	−	−
212	2	1	− 1	−	−	−
112	−	−	−	1	0	− 1
022	−	−	−	1	0	− 1
202	−	−	−	1	0	− 1

Table 10 Error evaluation of the approximate full adder

ATFA	NED	Delay × NED (E-12)	Power × NED (E-06)	PDP × NED (E-17)	EDP × NED (E-32)
proposed ATFA	0.0412	0.3321	0.4789	0.3860	0.3112
ATFA1 in [28]	0.0324	1.0682	0.7943	2.6189	8.6345
ATFA2 in [28]	0.037	1.2418	0.9093	3.0521	10.243
ATFA in [10]	0.037	0.6203	0.8656	1.4512	2.4330
ATFA2 in [21]	0.0275	0.2738	0.4926	0.4905	0.4884

and analysis parameters is better optimized in the proposed ATFA design, making it more efficient and less prone to errors.

$$\begin{aligned} \text{MED}_{\text{Cout}} &= \sum_{i=1}^{27} E D_i = |1 - 0| + |1 - 0| + |1 - 0| + |0 - 1| + |2 - 1| + |2 - 1| \\ &= 6/27 = 0.22 \end{aligned} \quad (18)$$

$$\begin{aligned} \text{MED}_{\text{SUM}} &= \sum_{i=1}^{27} E D_i = |0 - 2| + |0 - 2| + |0 - 2| + |1 - 0| + |1 - 0| + |1 - 0| \\ &= 9/27 = 0.33 \end{aligned} \quad (19)$$

$$\text{NED} = \text{MED}/\text{MAX} = 0.33/8 = 0.0412 \quad (20)$$

4.5 Application: Image Blending

The proposed ATFA's performance in image processing applications needs to be evaluated, given the widespread use of approximate adders in image and signal processing. In this study, we used the image blending application to simulate an 8-bit Ripple Carry Adder (RCA) in MATLAB software. We used four ATFA cells in the smaller half and four TFA cells in the more significant half of the adder. The image blend program blended two input images using a variable blending ratio α , producing an output image (Fig. 11). The value of α can be between zero and one, with values closer to one, indicating that the output image is more influenced by I_1 than I_2 . The output image is formed based on Eq. (21).

$$I_3 = I_1 \alpha + I_2 (1 - \alpha) \quad (21)$$

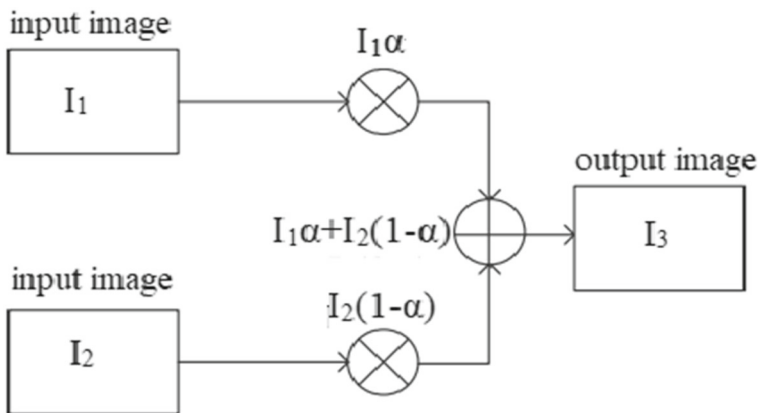


Fig. 11 image blending block diagram

In this program, the grayscale images' pixels are 8-bit unsigned binary digits. We used ATFA and TFA in MATLAB software to blend two grayscale images using blending ratios of 0.2, 0.6, and 0.8. We evaluated the output images' quality with respect to Peak Signal-to-Noise Ratio (PSNR), Structural Similarity Index Metric (SSIM), and Figure Of Merit (FOM) image quality criteria. Formulas discussed in Eqs. (22, 23, 24, 25, 26) are used in this study.

$$MSE = \frac{1}{mp} \sum_{i=0}^{m-1} \sum_{j=1}^{p-1} [I(i, j) - K(i, j)]^2 \quad (22)$$

$$PSNR = 10 \log_{10} \left(\frac{MAX_I^2}{MSE} \right) \quad (23)$$

The grayscale images are comprised of 8-bit unsigned binary digits. Using the ATFA and TFA within MATLAB software, two grayscale images are combined with blending ratios of 0.2, 0.6, and 0.8. The output images are evaluated with PSNR, SSIM, and FOM image quality criteria. FOM includes criteria for level, delay, and power. The results of the evaluations are recorded in Table 11, and the visual results are presented in Fig. 12. The obtained results based on formulas 24–28 are provided in Table 11. They indicate that the proposed ATFA has the lowest FOM values and performs better when balancing transistor parameters and approximate calculations.

$$SSIM(x, y) = \frac{(2\mu_x\mu_y + C_1) + (2\sigma_{xy} + C_2)}{(\mu_x^2 + \mu_y^2 + C_1)(\sigma_x^2 + \sigma_y^2 + C_1)} \quad (24)$$

$$MSSIM(x, y) = \frac{1}{M} \sum_{j=1}^M SSIM(x, y) \quad (25)$$

$$FOM1 = \frac{\text{Power} \times \text{Delay} \times \text{Area}}{PSNR} \quad (26)$$

$$FOM2 = \frac{\text{Power} \times \text{Delay} \times \text{Area}}{SSIM} \quad (27)$$

$$FOM3 = \frac{\text{Power} \times \text{Delay} \times \text{Area}}{SSIM \times PSNR} \quad (28)$$

As Table 11 shows, FOM criteria establish a balance between accuracy and other transistor parameters such as power consumption, delay, and area. From this perspective, the superiority of the proposed ATFA over other ATFA circuits is highly significant. According to Fig. 12, there are no significant differences between the images. Utilizing approximate circuits in systems that have the capability of tolerating faults can lead to improved parameters of transistor circuits.

Table 11 PSNR (dB), SSIM, and figures of merit (FOM)

Approximate TFA	ATFA1 in [28]	ATFA2 in [28]	ATFA in [10]	ATFA2 in [21]	The proposed design
<i>PSNR</i>					
0.2	36.2794	33.5152	33.6788	37.4783	33.0425
0.6	34.9019	33.9149	33.8391	35.0379	33.6245
0.8	36.212	34.6901	34.9923	37.9232	33.4834
<i>SSIN</i>					
0.2	0.9383	0.8969	0.8938	0.9413	0.8939
0.6	0.9032	0.8721	0.8811	0.9119	0.8745
0.8	0.9012	0.8723	0.8715	0.9204	0.8689
<i>FOM1</i>					
0.2	35.8930	47.0593	15.0588	5.0643	2.1441
0.6	37.3097	46.5047	14.9875	5.4170	2.1070
0.8	35.9598	45.4655	14.4936	5.0049	2.1158
<i>FOM2</i>					
0.2	1387.807	1758.505	567.4256	201.6400	79.2561
0.6	1441.740	1808.512	575.6043	208.1410	81.0143
0.8	1444.939	1808.097	581.9449	206.2188	81.5364
<i>FOM3</i>					
0.2	38.2533	52.4688	16.8481	5.3801	2.3986
0.6	41.3083	53.3249	17.0100	5.9404	2.4093
0.8	39.9022	52.1214	16.6306	5.4378	2.4351

5 Conclusion

The escalating usage of portable electronic equipment necessitates the need for high-performing batteries that exhibit low energy consumption. An efficacious approach to overcome common limitations in power management, signal delay and area is through utilization of approximate calculations and Ternary logic. In particular, Full Adder circuits play a crucial role in enhancing digital system output yield. Our novel ATFA design is poised to lead system-level improvements in facilitating the aforementioned criteria. To this end, this architecture employs advanced switching logic, in conjunction with pass transistors (PTLs) and transfer gates (TGATES) to harness higher performance with considerably alleviated delays, PDP, EDP, and relatively reduced circuit area. Transient Monte Carlo (MC) analysis conclusively confirms the proposed ATFA's unwavering robustness, even when nanotube diameter variation becomes apparent. Additionally, image blending simulations demonstrate the clear superiority of our proposed ATFA, with definitive superiorities for PSNR, SSIM, and Figure of Merit comparisons relative to its counterparts.

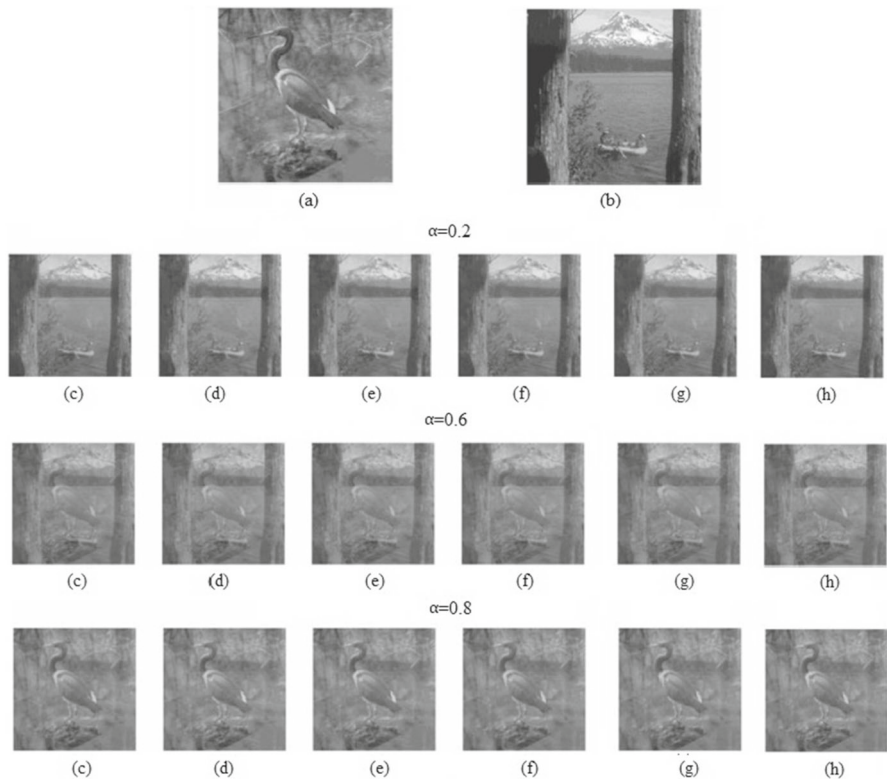


Fig. 12 The results of blending images of MATLAB software **a** input image1. **b** input image2. **c** exact image. **d** proposed ATFA. **e** The first ATFA of [28]. **f** The second ATFA of [28]. **g** The ATFA of [10]. **h** The second ATFA of [21]

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